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The Mars 2020 Lander Vision System: Architecture and I&T results

IPPW 2017

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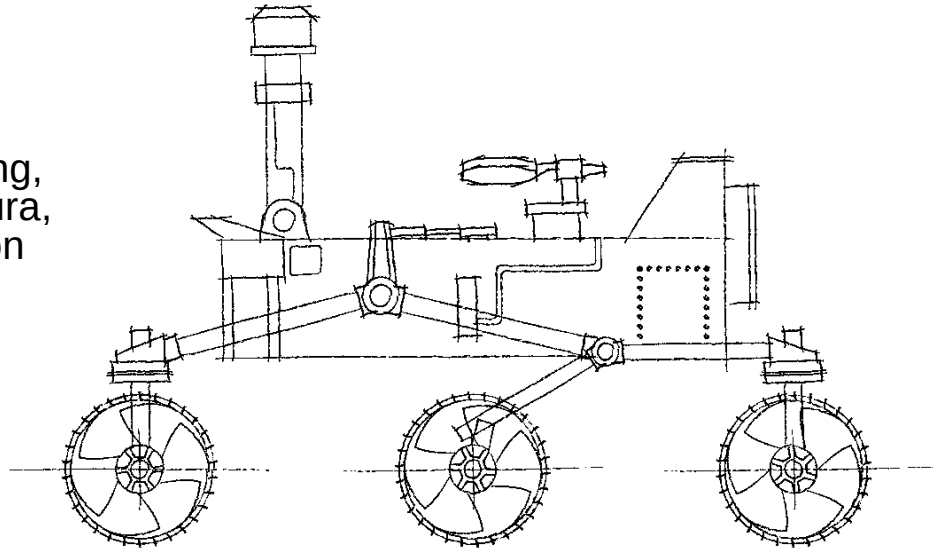
June 15, 2017



Mars 2020 Project

Terrain Relative Navigation

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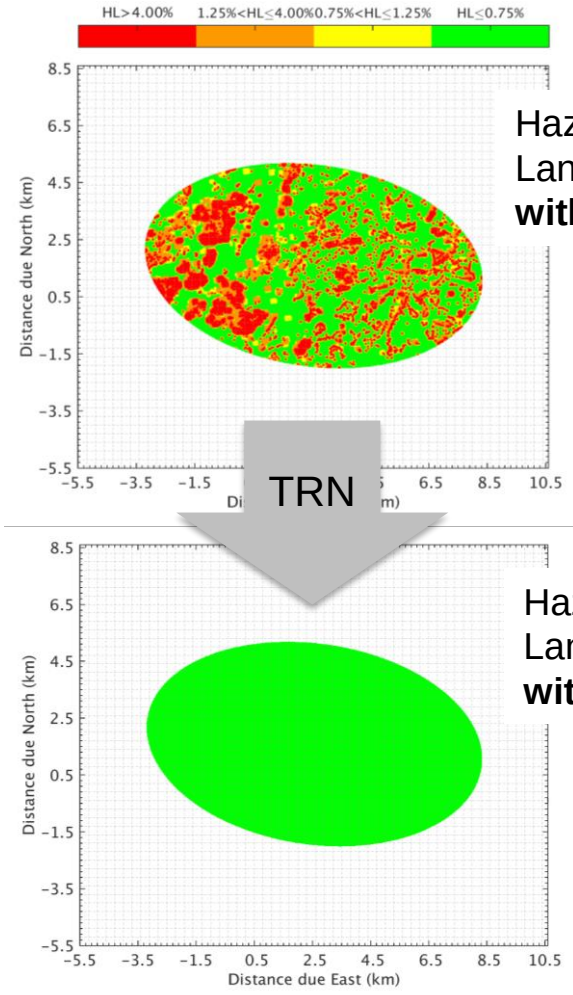
TRN enables access to hazardous landing sites

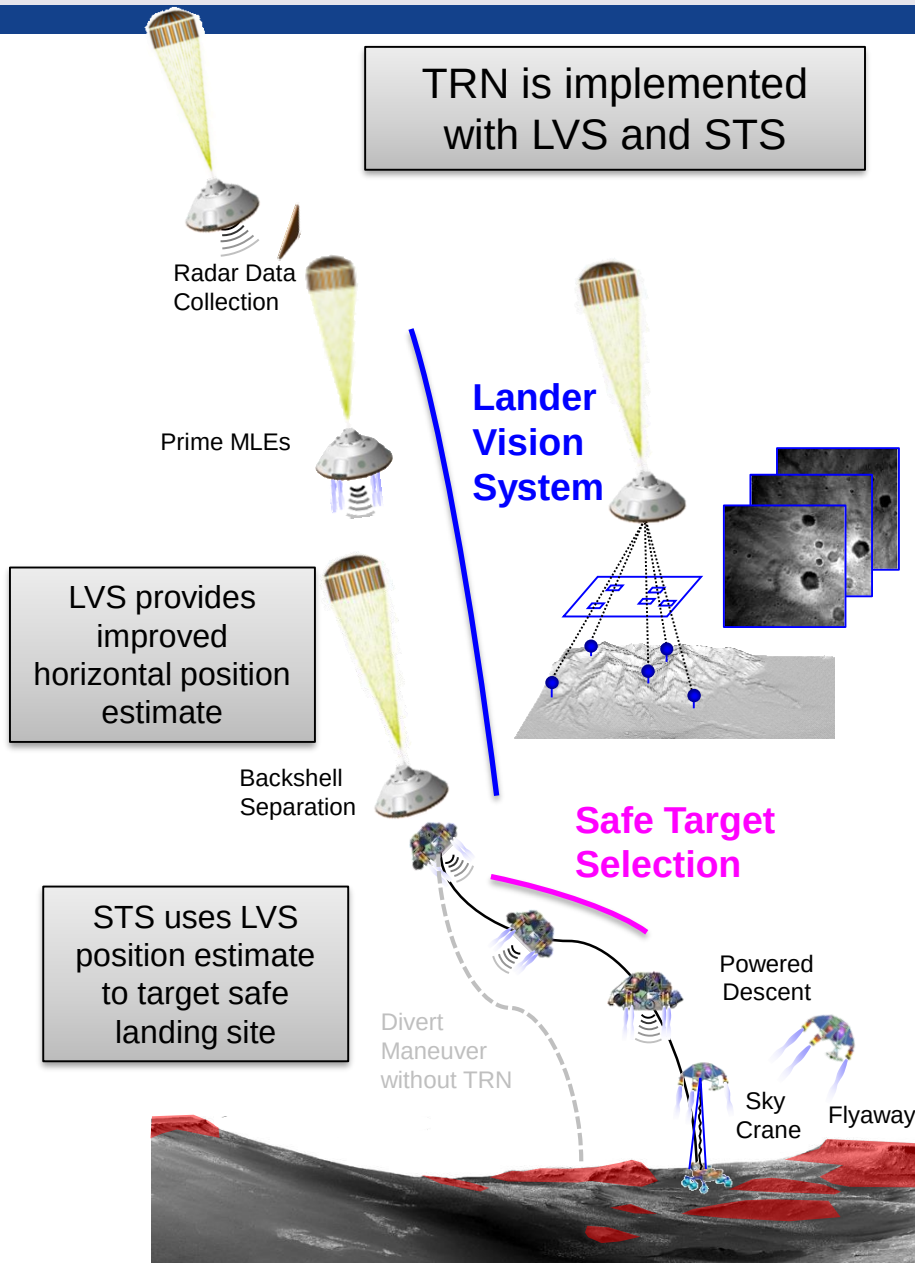


Hazards in Landing Ellipse **without TRN**

TRN

Hazards in Landing Ellipse **with TRN**

TRN is implemented with LVS and STS



Lander Vision System (LVS) Overview

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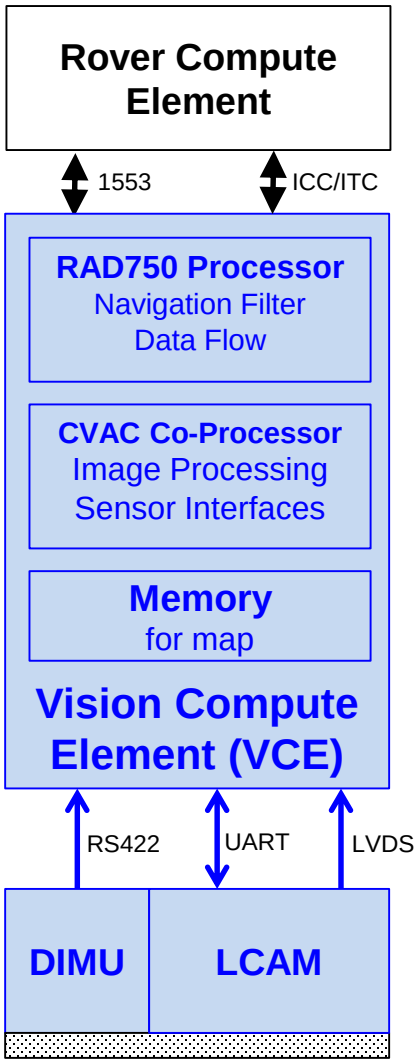

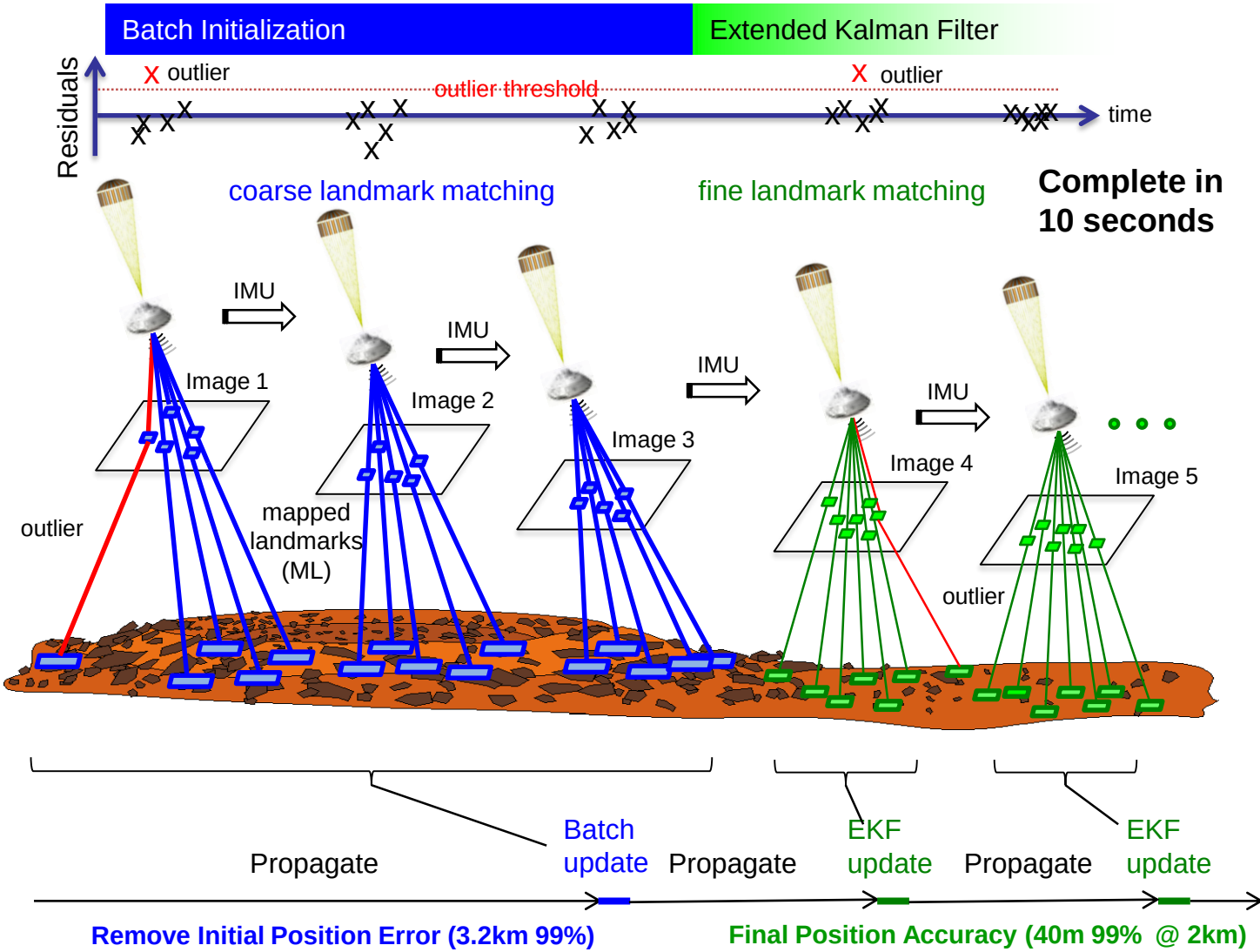

Vision Compute Element (VCE)

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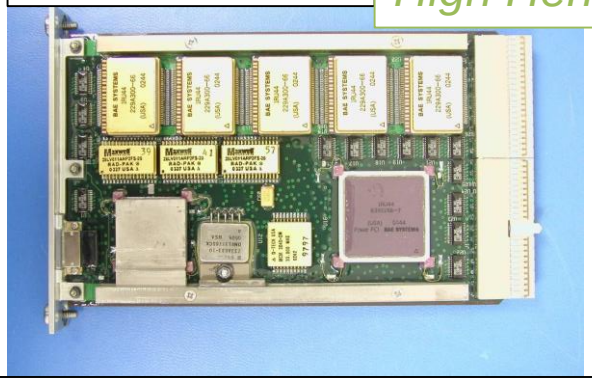
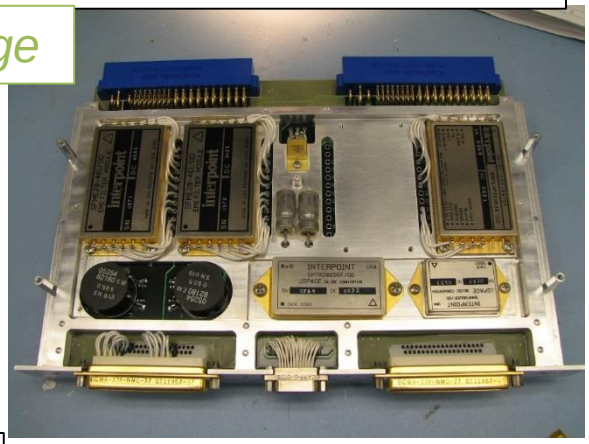
RAD750 Processor (3U) 132Mz Version

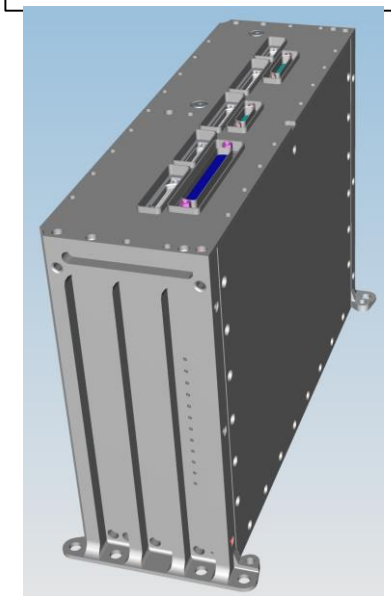


High Heritage

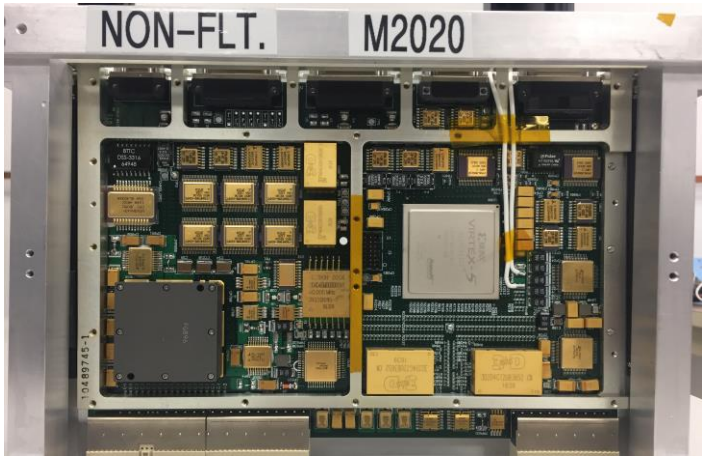
CEPCU1 power card (6U)



6U cPCI chassis and backplane



New Computer Vision Accelerator Card (CVAC) (6U)



The Vision Compute Element (VCE) is a 3 slot 6U processor with a RAD750 general purpose processor, a power conditioning card (CEPCU1) and a new Virtex5 enabled Computer Vision Accelerator Card (CVAC).

Lander Vision System Camera (LCAM)

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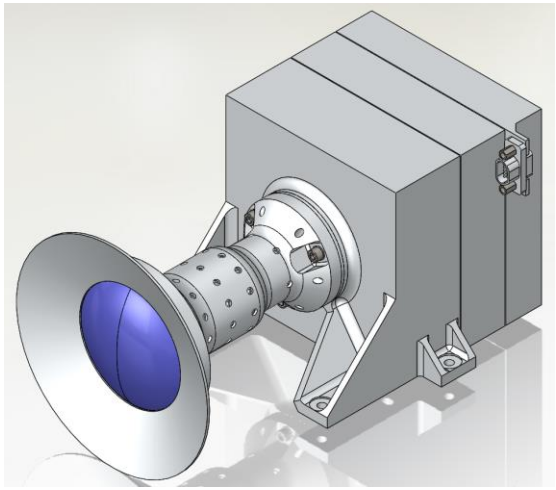
Parameter	Value
Detector Type	Global Shutter and Grayscale
Number of Pixels	1024 x 1024
Field of View	90˚ x 90˚
SNR	80 at half full-well depth
Exposure Time	~1ms
Latency	~100ms



- LCAM must take crisp images under high attitude rates and velocities
  - Requires global shutter with short exposure time
- LCAM must provide images to VCE quickly to meet LVS image processing requirements
  - Requires low image latency
- LCAM must provide images that ensure enough landmarks are matched per image
  - Requires large FOV to image significant map area even when camera pointed up to 45° off-nadir
- LCAM must provide high quality information across each landmark for accurate and robust landmark matching
  - Requires detector with large number of pixels and high image SNR

LVS Data Flow & Processing

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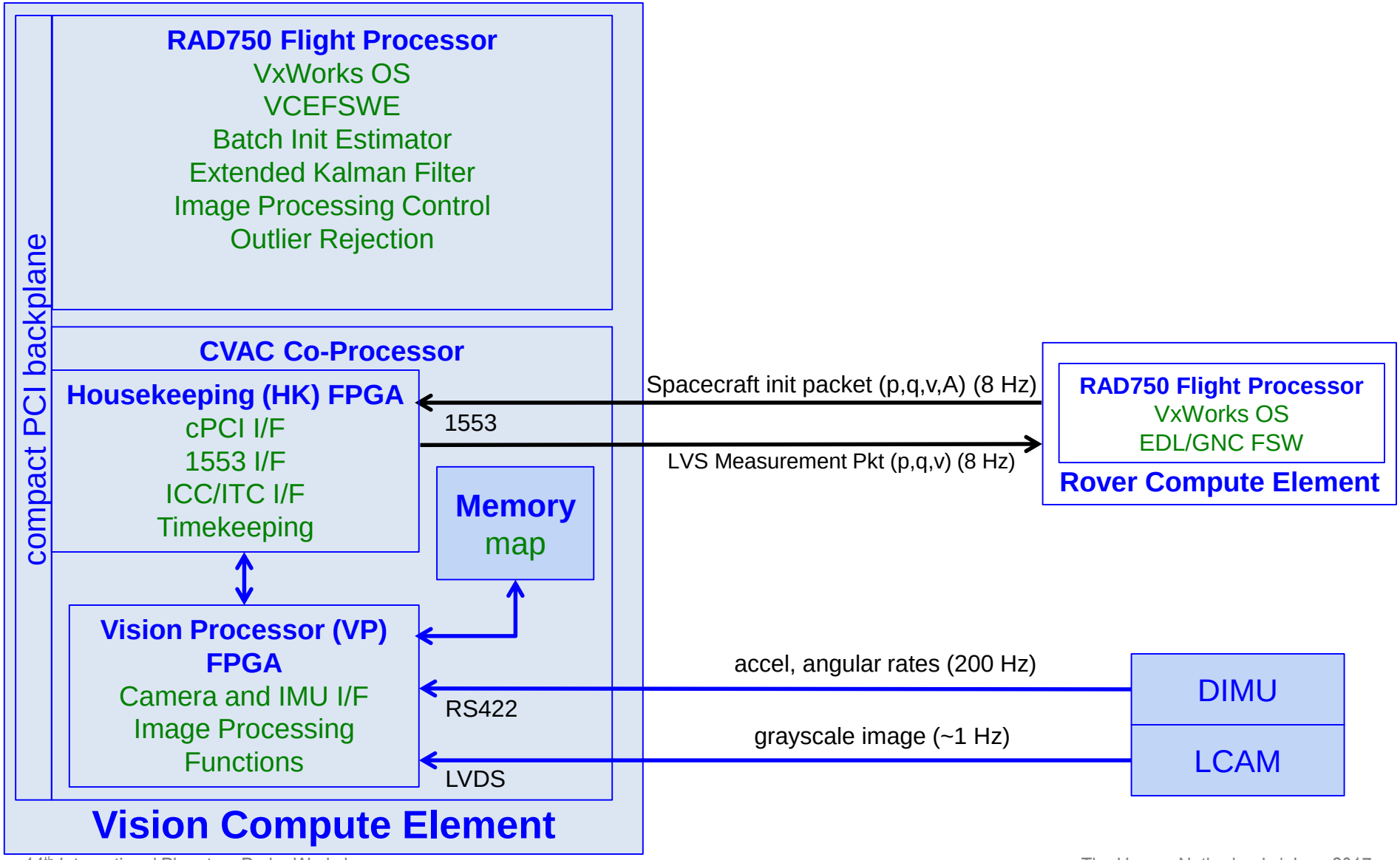

LVS Integration & Test Flow

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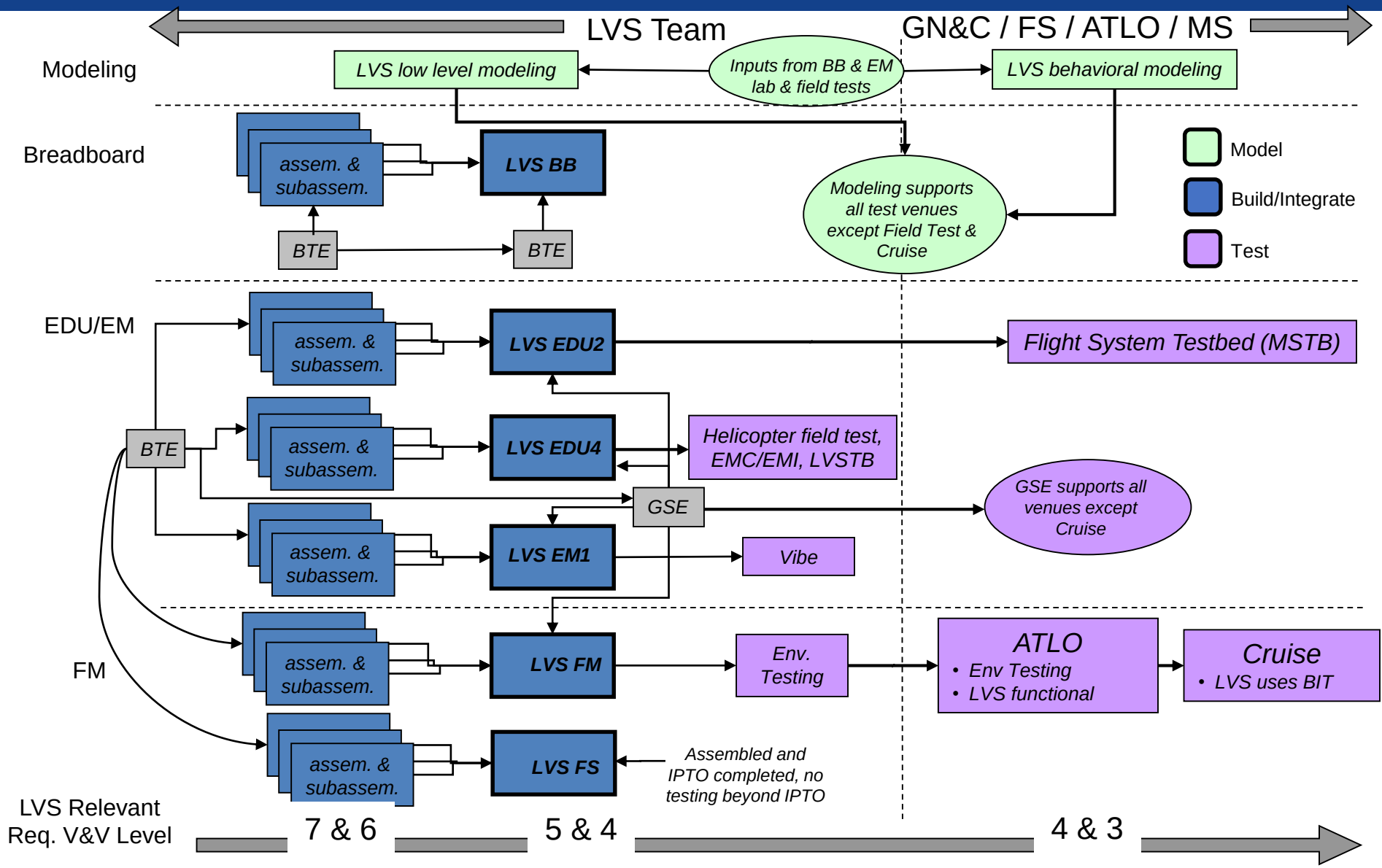
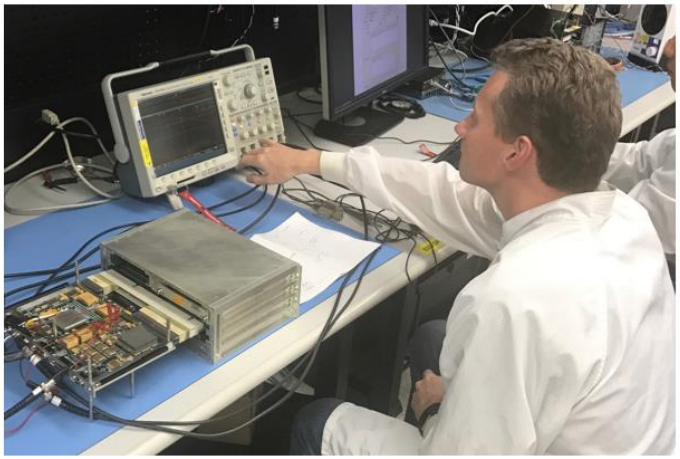


VCE I&T Status

- Breadboard
  - I&T complete
    - Initial testbed to develop test procedures and checkout CVAC design
    - Demonstrated that CVAC design is fundamentally sound
- EDU
  - I&T in progress
    - Completed majority of preliminary CVAC interface and functional tests
    - Detailed interface and functional tests continuing



VCEFSWE I&T Status

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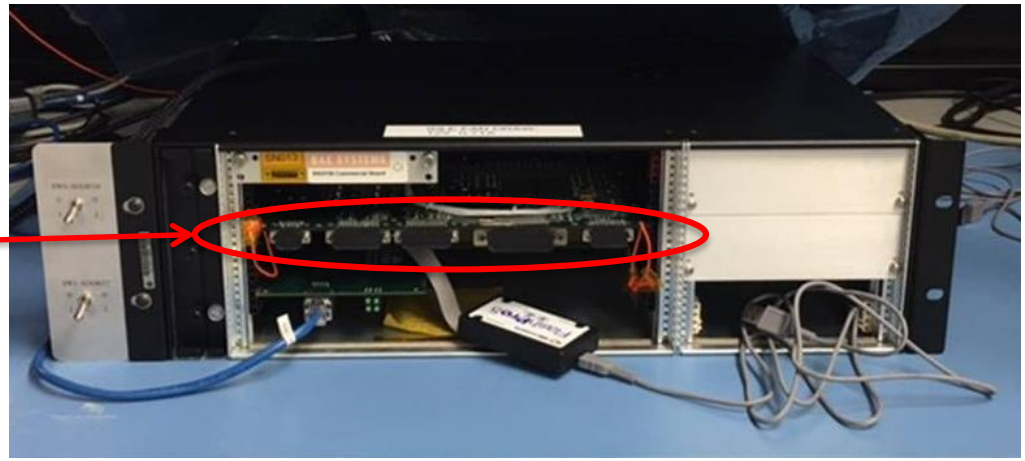
- Developed prototype that can execute end-to-end MRL sequence using VP functions on the VCE breadboard and EDU
  - Used canned input data for DIMU, LCAM and 1553 RT
  - Exercised coarse and fine mode IP functions in the VP FPGA
- Timing information provided key insights into improvements needed in the VP FPGA

- VCE CVAC Breadboard testbed
- No GSE sensor input supported



Key Upcoming LVS Milestones

- 2017
  - Continued LVS development activities; VCE, LCAM, VCEFSWE
- Q2 2018
  - EM VCE, EM DIMU, EM LCAM, VCEFSWE 2.0 delivered to LVS team
  - EM LVS I&T
- Q3 2018
  - EM LVS V&V
  - FM VCE, FM DIMU, FM LCAM, VCEFSWE 3.0 delivered to LVS team
  - FM LVS I&T/V&V
- Q4 2018
  - FM LVS delivered to ATLO

BACKUP

VCEFSWE and MRL Algorithms Data Flow

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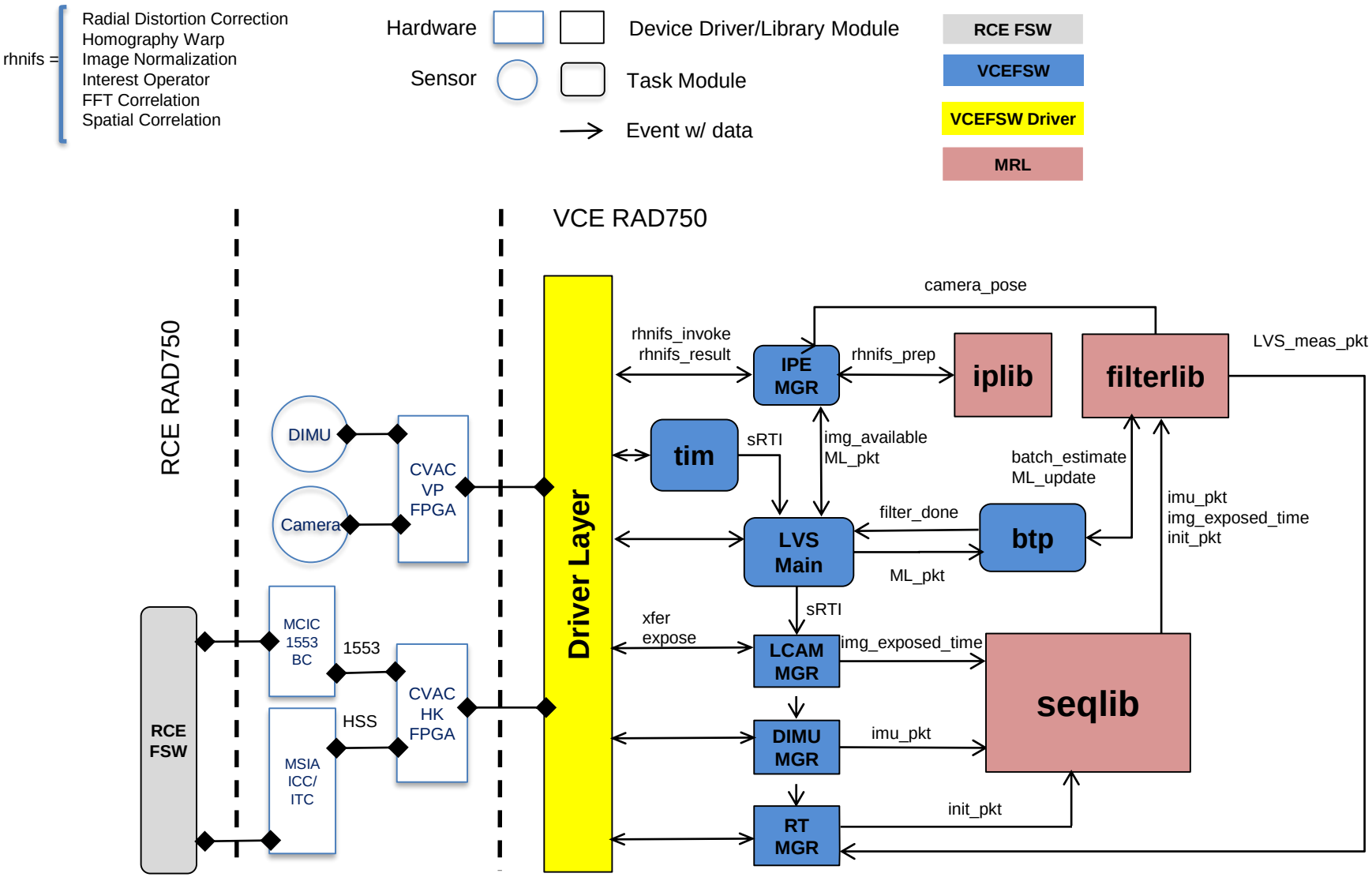

LVS I&T/V&V Venue Overview

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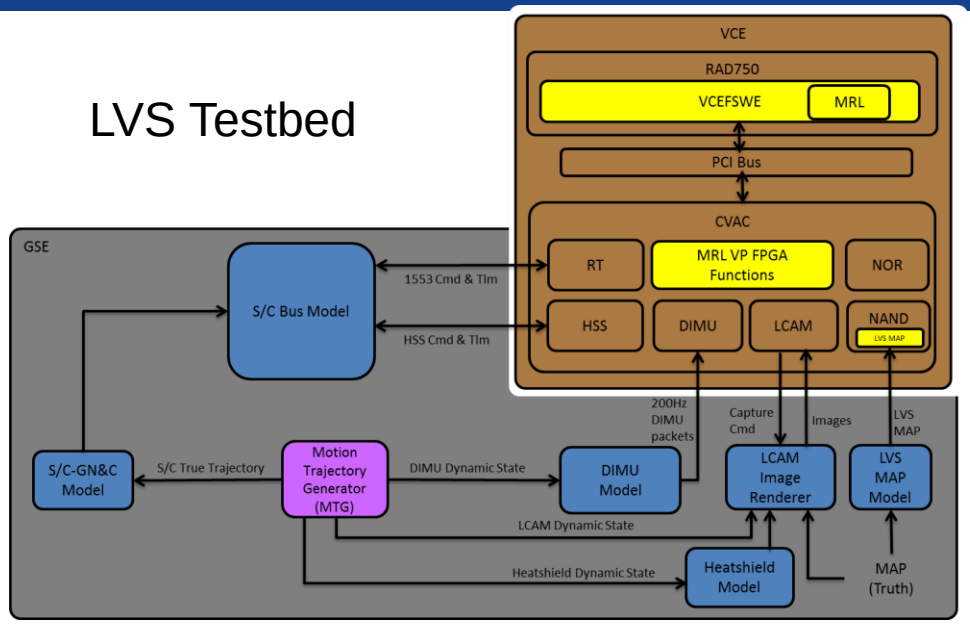
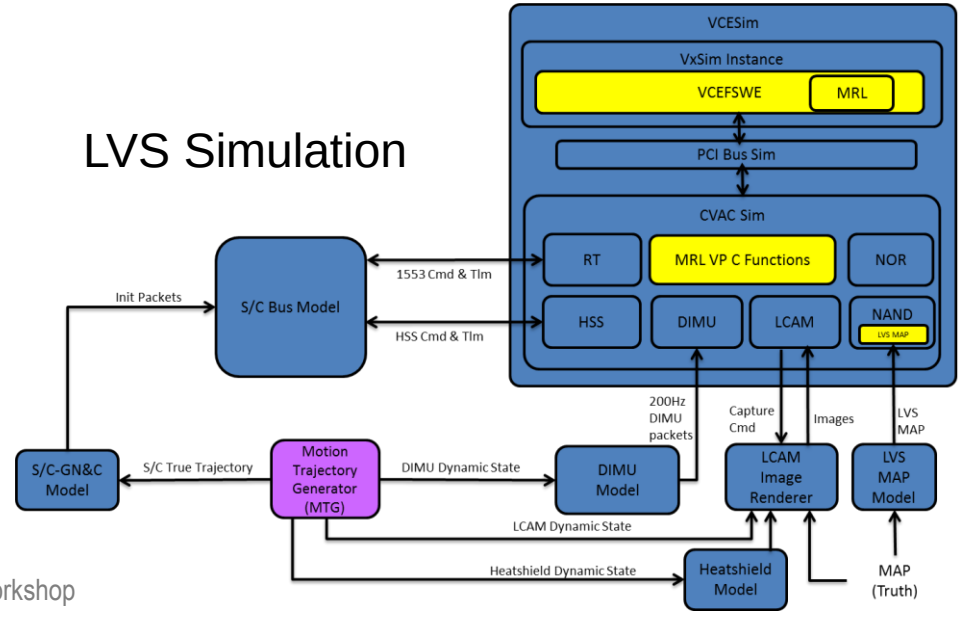
LVS Testbed



LVS Simulation

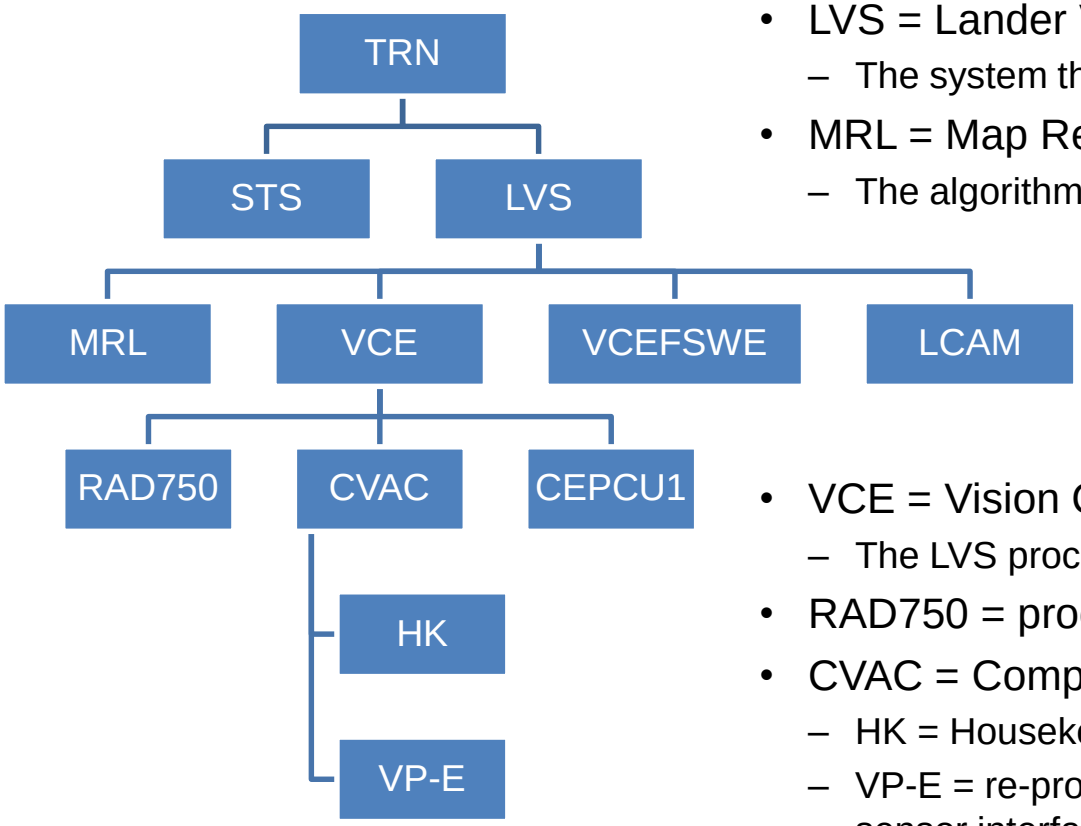


HW
SW
GSE
model
dynamics

Key Acronyms

- ATLO assembly, test, launch operations
- BB breadboard
- BIT built-in test
- CEPCU compute element power conditioning unit
- CVAC computer vision accelerator card
- DIMU descent inertial measurement unit
- EDL entry, descent, and landing
- EDU engineering development unit
- EM engineering model
- EMC electromagnetic compatibility
- EMI electromagnetic interference
- FM flight model
- FOV field of view
- FPGA field programmable gate array
- GNC guidance, navigation and control
- GSE ground support equipment
- HK housekeeping (RTAX 2000) FPGA)
- I&T integration and test
- IP image processing
- LCAM LVS camera
- LVS lander vision system
- LVSS LVS simulation
- LVSTB LVS test bed
- MRL map relative localization
- RCE rover compute element
- RT remote terminal
- SNR signal to noise ratio
- VCE vision compute element
- VCEFSW VCE flight software
- VP vision processor (Virtex 5) FPGA
- V&V verification and validation

Terminology



- TRN = Terrain Relative Navigation
  - All the new development to avoid known hazards in the landing ellipse
- STS = Safe Target Selection
  - Picks the safe landing site between a-priori hazards based on the position provided by LVS
- LVS = Lander Vision System
  - The system that performs Map Relative Localization
- MRL = Map Relative Localization
  - The algorithms that compute position relative to a map

- VCE = Vision Compute Element
  - The LVS processor containing three cards
- RAD750 = processor card
- CVAC = Computer Vision Accelerator Card
  - HK = Housekeeping FPGA on CVAC
  - VP-E = re-programmable Virtex5 FPGA on CVAC with sensor interfaces and image processing
- CEPCU1 = power conditioning card
- VCEFSWE = VCE Flight Software for EDL
- LCAM = LVS Camera, procured from MSSS